SPECIFICATIONS

CIO-DAS1601/12
CIO-DAS1602/12
CIO-DAS1602/16

Analog I/O & Digital I/O

Revision 6, November, 2000

A. CIO-DAS1601/12 & CIO-DAS1602/12

Power consumption

+5V	1.4 A typical, 2.1 A maximum

Analog input section

A/D converter type	ADS7800 successive approximation
Resolution	12 bits
Programmable ranges	
CIO-DAS1601/12	±10V, ±1V, ±0.1V, ±0.01V, 0 to 10V, 0 to 1V, 0 to 0.1V, 0 to 0.01V
CIO-DAS1602/12	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: external source (Din0, positive edge) or internal counter (positive or negative edge, jumper-select able) or software-polled
Burstmode	4 µs
Data transfer	From 512 sample FIFO via interrupt, DMA, DT-Connect to external memory board or software-polled
Polarity	Unipolar/Bipolar, switch selectable
Number of channels	8 differential or 16 single-ended, switch-selectable
Interrupts	2 to 7
Interrupt enable	Programmable
Interrupt sources	End-of-conversion, terminal count (DMA)
DMA	Channel 1 or 3
Trigger sources	External hardware/software (DIn0)
A/D conversion time	3.3 µs
Throughput	
DMA	160 kHz
DT-Connect (multi-channel)	250 kHz
DT-Connect (single-channel)	330 kHz
Differential Linearity error	±1 LSB
Integral Linearity error	±1 LSB
No missing codes guaranteed	12 bits
Gain drift	±60 ppm/°C
Zero drift	±160 ppm/°C
Input leakage current (@25 Deg C)	200 nA
Input impedance	10 Megohms minimum
Absolute maximum input voltage	±35V

Analog Output:

Resolution	12 bits
Number of channels	2
D/A type	MX7548
Voltage Ranges	±10V, ±5V, 0 to 5V, 0 to 10V or user defined range between 0 and 10V. Each channel independently configurable by jumpers.
Offset error	Trimmable to 0 by potentiometer
Gain error	Trimmable to 0 by potentiometer
Differential nonlinearity	±1 LSB maximum
Integral nonlinearity	±1 LSB maximum
Monotonicity	Guaranteed monotonic
D/A pacing	Software paced
Data transfer	Double buffered software transfer, update on write to MSB register.
Throughput	System dependent, software paced.
Slew Rate	0.3V/µs
Current Drive (OP07)	±5 mA minimum
Output short-circuit duration	Indefinite
Output coupling	DC
Output impedance	0.1 Ohms maximum
Miscellaneous	Double-buffered output latches

Digital Input / Output

Digital Type (Digital I/O connector)	82C55 (not applicable on -P5 versions)
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts minimum @ –2.5 mA
Output Low	0.4 volts maximum @ 2.5 mA
Input High	2.0 volts minimum, 5.5 volts absolute max
Input Low	0.8 volts maximum, –0.5 volts absolute minimum
Digital Type (Main analog connector)	
Output	74LS197
Input	74LS244
Configuration	4 fixed input, 4 fixed output
Number of channels	8
Output High	2.7 volts minimum @ –0.4 mA
Output Low	0.5 volts maximum @ 8 mA
Input High	2.0 volts minimum, 7 volts absolute maximum
Input Low	0.8 volts max, –0.5 volts absolute minimum

Counter Section

Counter type	82C54
Configuration	3 down-counters, 16 bits each
	Counter 0 - Independent, user configurable
	Source: Programmable - Internal 100 kHz or external (CTR0 Clock In)
	Gate: External (DIn2)
	Output: Available at user connector (CTR0 Out)
	Counter 1 - ADC Pacer Lower Divider
	Source: 1 or 10 MHz oscillator (jumper selectable)
	Gate: Tied to Counter 2 gate, programmable source.
	Output: Chained to Counter 2 Clock.
	Counter 2 - ADC Pacer Upper Divider
	Source: Counter 1 Output.
	Gate: Tied to Counter 1 gate, programmable source.
	Output: ADC Pacer clock

Clock input frequency	10 MHz maximum
High pulse width (clock input)	30 ns minimum
Low pulse width (clock input)	50 ns minimum
Gate width high	50 ns minimum
Gate width low	50 ns minimum
Input low voltage	0.8V maximum
Input high voltage	2.0V minimum
Output low voltage	0.4V maximum
Output high voltage	3.0V minimum

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	–20 to 70°C
Humidity	0 to 90% non-condensing
Weight	1.2 oz. (320g)

B. CIO-DAS1602/16

Power consumption

+5	1.4 A typical, 2.1 A maximum

Analog input section

A/D converter type	ADS7805 successive approximation
Resolution	16 bits
Programmable ranges	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: external source (Din0, positive edge) or internal counter (positive or negative edge, jumper-select able) or software-polled
Burstmode	13.3 µs
Data transfer	From 512-sample FIFO via interrupt, DMA, DT-Connect to external memory board or software polled

Polarity	Unipolar/Bipolar, switch selectable
Number of channels	8 differential or 16 single-ended, switch-selectable
Interrupts	2 to 7
Interrupt enable	Programmable
Interrupt sources	End-of-conversion, terminal count (DMA)
DMA	Channel 1 or 3
Trigger sources	External hardware/software (DIn0)
A/D conversion time	10 µs
Throughput	100 kHz
Differential Linearity error (Bipolar)	±1 LSB
Integral Linearity error (Bipolar)	±1.5 LSB
No missing codes guaranteed	16 bits
Gain drift	±7 ppm/°C
Zero drift	±2 ppm/°C
Input leakage current (@25 Deg C)	200 nA
Input impedance	10 MegOhms minimum
Absolute maximum input voltage	±35V

Analog Output:

Resolution	12 bits
Number of channels	2
D/A type	MX7548
Voltage Ranges	±10V, ±5V, 0 to 5V, 0 to 10V or user-defined range between 0 and 10V. Each channel independently configurable by jumpers.
Offset error	Trimmable to 0 by potentiometer
Gain error	Trimmable to 0 by potentiometer
Differential nonlinearity	±1LSB maximum
Integral nonlinearity	±1LSB maximum
Monotonicity	Guaranteed monotonic
D/A pacing	Software paced
Data transfer	Double-buffered software transfer, update on write to MSB register.
Throughput	System-dependent, software-paced.
Slew Rate	0.3V/µs
Current Drive (OP07)	±5 mA minimum
Output short-circuit duration	Indefinite
Output coupling	DC
Output impedance	0.1 ohms maximum
Miscellaneous	Double-buffered output latches

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  - Gate: Tied to Counter 2 gate, programmable source.
  - Output: Chained to Counter 2 Clock.
- Counter 2 - ADC Pacer Upper Divider
  - Source: Counter 1 Output.
  - Gate: Tied to Counter 1 gate, programmable source.
  - Output: ADC Pacer clock

Clock input frequency	10 MHz maximum
High pulse width (clock input)	30 ns minimum
Low pulse width (clock input)	50 ns minimum
Gate width high	50 ns minimum
Gate width low	50 ns minimum
Input low voltage	0.8V maximum
Input high voltage	2.0V minimum
Output low voltage	0.4V maximum
Output high voltage	3.0V minimum

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	20 to 70°C
Humidity	0 to 90% non-condensing

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