Specifications

PCI-2515

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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	Successive approximation
Resolution	16-bits
Number of channels	16 single-ended/8 differential, software selectable
Input ranges (SW programmable)	Bipolar: ±10 V, ±5 V, ±2 V, ±1 V , ±0.5 V, ±0.2 V, ±0.1 V
Maximum sample rate	1 MHz
Nonlinearity (integral)	±2 LSB maximum
Nonlinearity (differential)	±1 LSB maximum
A/D pacing	Onboard A/D clock, external source (XAPCR)
Trigger sources and modes	See Table 7
Data transfer	DMA
Configuration memory	Programmable I/O
Maximum usable input voltage + common mode voltage (CMV + V_{in})	Range: ±10 V, ±5 V, ±2 V, ±1 V , ±0.5 V 10.5 V maximum Range: ±0.2 V, ±0.1 V 2.1 V maximum
Signal to noise and distortion	*72 dB typical for ±10 V range, 1 kHz fundamental*
Total harmonic distortion	*-80 dB typical for ±10 V range, 1 kHz fundamental*
Calibration	Auto-calibration, calibration factors for each range stored onboard in non-volatile RAM.
CMRR @ 60 Hz	-70 dB typical DC to 1 kHz
Bias current	*40 pA typical (0°C to 35°C)*
Input impedance	*10 MΩ single-ended, 20 MΩ differential*
Absolute maximum input voltage	*±30 V*

Accuracy

Table 2. Analog input accuracy specifications

Voltage range		**Accuracy ±(% of reading + % range) 23°C ±10 °C, 1 year**	**Temperature coefficient ±(ppm of reading + ppm range)/°C**	***Noise (cts RMS)***	
-10 V to 10 V	Note 1	0.031% + 0.008%	14 + 8	*1.5*	*Note 2*
-5 V to 5 V		0.031% + 0.009%	14 + 9	*2.0*	
-2 V to 2 V		0.031% + 0.010%	14 +10	*1.6*	
-1 V to 1 V		0.031% + 0.02%	14 + 12	*2.5*	
-500 mV to 500 mV		0.031% + 0.04%	14 +18	*4.0*	
-200 mV to 200 mV		0.036% + 0.075%	14 +12	*5.0*	
-100 mV to 100 mV		0.042% + 0.15%	14 +18	*9.0*	

Note 1: Specifications assume differential input single-channel scan, 1 MHz scan rate, unfiltered, CMV=0.0 V, 30 minute warm-up, exclusive of noise.

Note 2: Noise reflects 10,000 samples at 1 MHz, typical, differential short, using CA-68-3S cable.

Analog outputs

Analog output channels can be updated synchronously relative to scanned inputs, and clocked from either an internal onboard clock, or an external clock source. Analog outputs can also be updated asynchronously, independent of any other scanning system.

Table 3. Analog output specifications

Channels	2
Resolution	16-bits
Data buffer	PC-based memory
Output voltage range	±10 V
Output current	±10 mA
Offset error	±0.0045 V maximum
Digital feed-through	<10 mV when updated
DAC analog glitch	<12 mV typical at major carry
Gain error	±0.01%
Coupling	DC
Update rate	1 MHz maximum, resolution 20.83 ns
Settling time	2 µs to rated accuracy
Pacer sources	Four programmable sources: ▪ Onboard D/A clock, independent of scanning input clock ▪ Onboard scanning input clock ▪ External D/A input clock, independent of external scanning input clock-(XDPCR) ▪ External scanning input clock-(XAPCR)
Trigger sources	Start of input scan

Digital input/output

Table 4. Digital input/output specifications

Number of I/O	24
Ports	Three banks of 8. Each port is programmable as input or output
Input scanning mode	*Asynchronous, under program control at any time relative to input scanning*
Configuration	10 kΩ pull-up to +5 V, 20 pf to analog common
Input protection	±15 kV ESD clamp diodes
Input high	*+2.0 V to +5.0 V*
Input low	*0 to 0.8 V*
Output high	*>2.0 V*
Output low	*<0.8 V*
Output current	Output 12 mA per pin, 200 mA total continuous
Digital input pacing	Onboard clock, external clock (XAPCR)
Digital output pacing	Four programmable sources: ▪ Onboard D/A clock, independent of scanning input clock ▪ Onboard scanning input clock ▪ External D/A input clock, independent of external scanning input clock-(XDPCR) ▪ External scanning input clock-(XAPCR)
Digital input trigger sources and modes	See Table 7
Digital output trigger sources	Start of input scan
Data transfer	DMA
Sampling/update rate	12 MHz maximum
Pattern generation output	Two of the 8-bit ports can be configured for 16-bit pattern generation. The pattern can also be updated synchronously with an acquisition at up to 12 MHz.

Counters

Counter inputs can be scanned based on an internal programmable timer or an external clock source.

Table 5. Counter specifications

Channels	4 independent
Resolution	32-bit
Input frequency	20 MHz maximum
Input signal range	-5 V to 10 V
Input characteristics	10 kΩ pull-up, ±15 kV ESD protection
Trigger level	TTL
Minimum pulse width	25 ns high, 25 ns low
De-bounce times	16 selections from 500 ns to 25.5 ms, positive or negative edge sensitive, glitch detect mode or de-bounce mode
Time-base accuracy	30 ppm (0 ° to 50 °C)
Counter read pacer	Onboard clock, external clock (XAPCR)
Trigger sources and modes	See Table 7
Programmable mode	Counter
Counter mode options	Totalize, clear on read, rollover, stop at all Fs, 16-bit or 32-bit, any other channel can gate the counter

Input sequencer

Analog, digital, and counter inputs can be scanned based on either an internal programmable timer or an external clock source.

Table 6. Input sequencer specifications

Scan clock sources: two (Note 3)	Internal: ▪ Analog channels from 1 µs to 1 sec in 20.83 ns steps. ▪ Digital channels and counters from 83.33 ns to 1 sec in 20.83 ns steps. External. TTL-level input: ▪ Analog channels down to 1 µs minimum ▪ Digital channels and counters down to 83 ns minimum
Programmable parameters per scan:	Programmable channels (random order), programmable gain
Depth	512 locations
Onboard channel-to-channel scan rate	Analog: 1 MHz maximum Digital: 12 MHz
External acquisition scan clock input maximum rate	1.0 MHz
Clock signal range:	Logical zero: 0 V to 0.8 V Logical one: 2.4 V to 5.0 V
Minimum pulse width	50 ns high, 50 ns low

Note 3: The maximum scan clock rate is the inverse of the minimum scan period. The minimum scan period is equal to 1 µs times the number of analog channels. If a scan contains only digital channels then the minimum scan period is 83 ns times the number of digital channels.

Trigger sources and modes

Table 7. Trigger sources and modes

Input scan trigger sources	▪ Single channel analog hardware trigger ▪ Single channel analog software trigger ▪ External-single channel digital trigger (TTL TRG input) ▪ Digital pattern trigger ▪ Counter/totalizer trigger
Input scan triggering modes	Single channel analog hardware trigger: The first analog input channel in the scan is the analog trigger channel. ▪ Input signal range: -10 V to +10 V maximum ▪ Trigger level: Programmable (12-bit resolution) ▪ Latency: 350 ns typical ▪ Accuracy: ±0.5% of reading, ±2 mV offset maximum ▪ Noise: 2 mV RMS typical
	Single channel analog software trigger: The first analog input channel in the scan is the analog trigger channel. ▪ Input signal range: Anywhere within range of the trigger channel ▪ Trigger level: Programmable (16-bit resolution) ▪ Latency: One scan period maximum
	External-single channel digital trigger (TTL trigger input): ▪ Input signal range: -15 V to +15 V maximum ▪ Trigger level: TTL-level sensitive ▪ Minimum pulse width: 50 ns high, 50 ns low ▪ Latency: One scan period maximum
	Digital pattern triggering: 8-bit or 16-bit pattern triggering on any of the digital ports. Programmable for trigger on equal, not equal, above, or below a value. Individual bits can be masked for "don't care" condition. Latency: One scan period maximum
	Counter/totalizer triggering: Counter/totalizer inputs can trigger an acquisition. User can select to trigger on a frequency or on total counts that are equal, not equal, above, or below a value, or within/outside of a window rising/falling edge. Latency: One scan period maximum

Frequency/pulse generators

Table 8. Frequency/pulse generator specifications

Channels	2 x 16-bit
Output waveform	Square wave
Output rate	1 MHz base rate divided by 1 to 65535 (programmable)
High-level output voltage	2.0 V minimum @ -1.0 mA, 2.9 V minimum @ -400 µA
Low-level output voltage	0.4 V maximum @ 400 µA

Power consumption

Table 9. Power consumption specifications

Power consumption (per board)	3 W

PCI compatibility

Table 10. PCI compatibility specifications

PCI bus	PCI r2.2 compliant, universal 3.3 V/5 V signaling support, compatible with PCI-X

Environmental

Table 11. Environmental specifications

Operating temperature range	0 to +60 °C
Storage temperature range	-40 to +80 °C
Relative humidity	0 to 95% non-condensing

Mechanical

Table 12. Mechanical specifications

Vibration	MIL STD 810E cat 1 and 10
Dimensions	165 mm (W) x 15 mm (D) x 108 mm (H) (6.5" x 0.6" x 4.2")
Weight	160 g (0.35 lbs)

Main connector and pin out

Table 13. Main connector specifications

Connector type	68-pin standard "SCSI TYPE III" female connector HDMI connector (targeted for future expansion)
Compatible cables (for the 68-pin SCSI connector)	CA-68-3R — 68-pin ribbon cable; 3 feet. CA-68-3S — 68-pin shielded round cable; 3 feet. CA-68-6S — 68-pin shielded round cable; 6 feet.
Compatible accessory products	TB-100 termination board with screw terminals
	RM-TB-100, 19-inch rack mount kit for TB-100

Table 14. 16-channel single-ended pin out

Pin	Function	Pin	Function
68	ACH0	34	ACH8
67	AGND	33	ACH1
66	ACH9	32	AGND
65	ACH2	31	ACH10
64	AGND	30	ACH3
63	ACH11	29	AGND
62	SGND (low level sense – not for general use)	28	ACH4
61	ACH12	27	AGND
60	ACH5	26	ACH13
59	AGND	25	ACH6
58	ACH14	24	AGND
57	ACH7	23	ACH15
56	NC	22	XDAC0
55	NC	21	XDAC1
54	NEGREF	20	POSREF
53	GND	19	+5 V (see Note 4)
52	A1	18	A0
51	A3	17	A2
50	A5	16	A4
49	A7	15	A6
48	B1	14	B0
47	B3	13	B2
46	B5	12	B4
45	B7	11	B6
44	C1	10	C0
43	C3	9	C2
42	C5	8	C4
41	C7	7	C6
40	GND	6	TTL TRG
39	CNT1	5	CNT0
38	CNT3	4	CNT2
37	TMR1	3	TMR0
36	GND	2	XAPCR

Table 15. 8-channel differential pin out

Pin	Function	Pin	Function
68	ACH0 HI	34	ACH0 LO
67	AGND	33	ACH1 HI
66	ACH1 LO	32	AGND
65	ACH2 HI	31	ACH2 LO
64	AGND	30	ACH3 HI
63	ACH3 LO	29	AGND
62	SGND (low level sense – not for general use)	28	ACH4 HI
61	ACH4 LO	27	AGND
60	ACH5 HI	26	ACH5 LO
59	AGND	25	ACH6 HI
58	ACH6 LO	24	AGND
57	ACH7 HI	23	ACH7 LO
56	NC	22	XDAC0
55	NC	21	XDAC1
54	NEGREF	20	POSREF
53	GND	19	+5 V (see Note 4)
52	A1	18	A0
51	A3	17	A2
50	A5	16	A4
49	A7	15	A6
48	B1	14	B0
47	B3	13	B2
46	B5	12	B4
45	B7	11	B6
44	C1	10	C0
43	C3	9	C2
42	C5	8	C4
41	C7	7	C6
40	GND	6	TTL TRG
39	CNT1	5	CNT0
38	CNT3	4	CNT2
37	TMR1	3	TMR0
36	GND	2	XAPCR

Note 4: 5 V output, up to 500 mA.

Measurement Computing Corporation
10 Commerce Way
Suite 1008
Norton, Massachusetts 02766
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@mccdaq.com
www.mccdaq.com