LGR-5325

Analog and Digital I/O Logger

User's Guide

MEASUREMENT COMPUTING™

LGR-5325

Analog and Digital I/O Logger

User's Guide

Document Revision 2, January, 2011
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Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide explains how to install and use the LGR-5325 so that you get the most out of its USB data acquisition features.

This user's guide also refers you to related documents available on our web site, and to technical support resources.

Conventions in this user's guide

For more information on …

Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

<#:#> Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.

bold text **Bold** text is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example:

1. Insert the disk or CD and click the **OK** button.

italic text *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example:

- The software installation procedure is explained in the *DAQLog Software User's Guide*
- *Never touch* the exposed pins or circuit connections on the board.

Introducing the LGR-5325

This user's guide contains all of the information you need to connect the LGR-5325 to your computer and to the signals you want to measure and log.

The LGR-5325 is a USB 2.0 full-speed device supported under popular Microsoft® Windows® operating systems. The LGR-5325 is compatible with both USB 1.1 and USB 2.0 ports.

With a multiplexed 16-bit A/D converter and a maximum sampling rate of 100 kS/s for all analog input channels, the LGR-5325 can sample:

- Up to 16 single-ended analog inputs
- Up to eight differential analog inputs
- In ranges of ±10 V, ±5 V, ±1 V

You can start an analog input scan by:

- Pressing **START**
- Configuring an external digital trigger
- Configuring an external analog trigger
- Configuring a digital pattern trigger
- Pressing **TRIG** to override a configured trigger

The LGR-5325 also has 16 digital input connections (TTL thresholds with 28 V tolerance) that you can configure to detect and log events based on change of state or pattern recognition..

The LGR-5325's single digital output is a 500 V alarm output implemented as a single Form C relay. You can configure the relay to energize when the trigger condition is met and data is being recorded.

The LGR-5325's four counter channels support the following counter modes:

- Counter (general event counting)
- Period counting
- Pulse width counting
- Edge-to-edge timing
- Up/down counting

You can use the Modulo N number and mode with all of the counter modes listed to determine how the counter behaves when it reaches the *modulo* number you set.

The device saves data to and retrieves data from a Secure Digital (SD) or Secure Digital High Capacity (SDHC) memory card. The LGR-5325 requires 9–30 VDC of external power.

The LGR-5325 is shown below. Use the two sets of screw terminals to make all I/O connections.

For information on the features of the DAQLog software included with your LGR-5325, refer to the *DAQLog Software User's Guide* that shipped with your device.

LGR-5325 block diagram

Figure 1 shows a simplified block diagram of the LGR-5325. This device provides all of the functional elements shown in the figure.

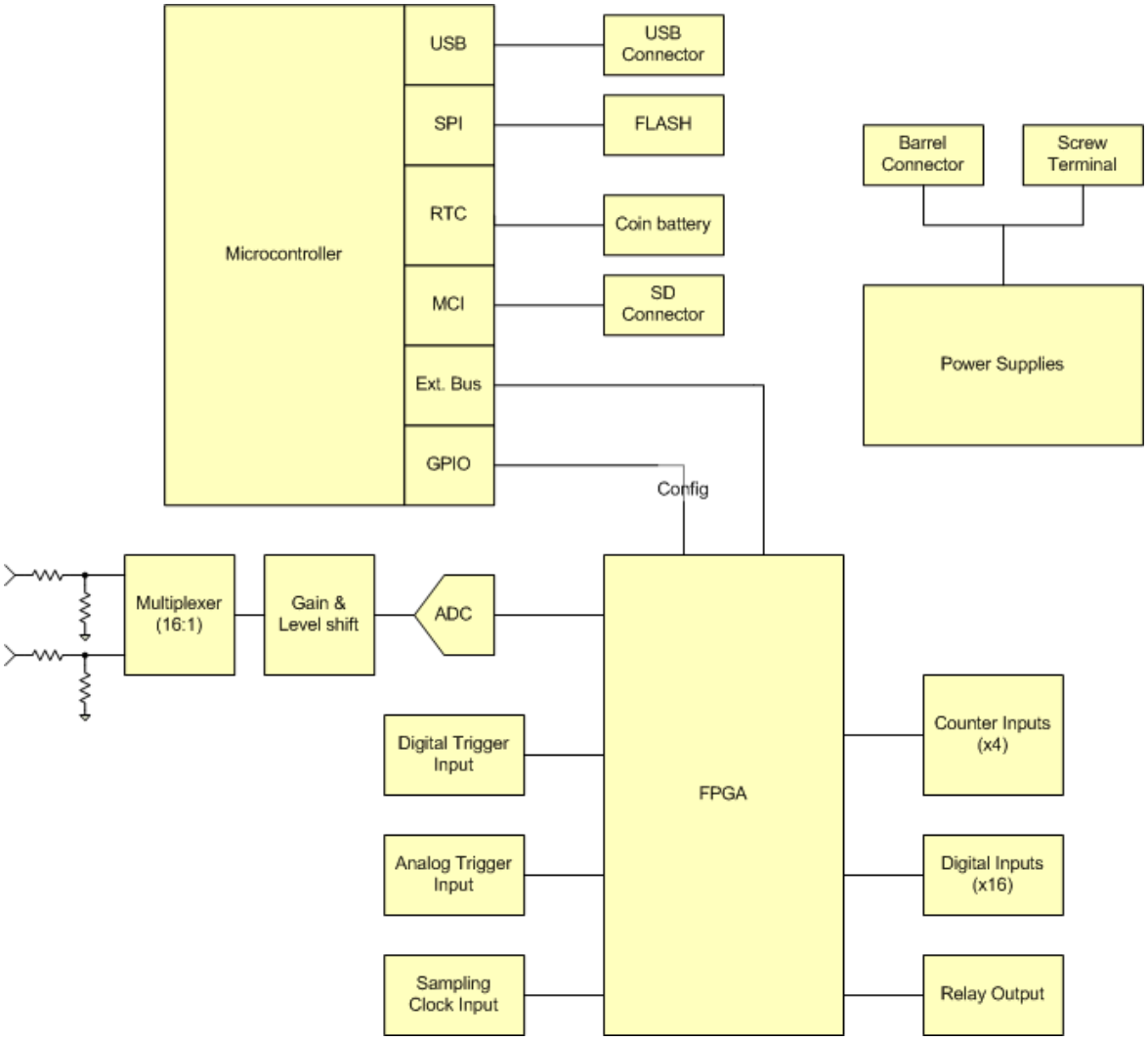

Figure 1. LGR-5325 functional block diagram

Getting Started with the LGR-5325

This document explains how to unpack, connect, and use the LGR-5325 to perform and log analog input scans, digital input scans, and counter operations.

Unpacking the LGR-5325

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the LGR-5325 from its packaging, ground yourself using a wrist strap, or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If your LGR-5325 is damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail. For international customers, contact your local distributor where you purchased the LGR-5325.

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

What comes with your LGR-5325 shipment?

As you unpack your LGR-5325, verify that the following components are included.

Hardware

- LGR-5325

- USB cable (2-meter length)

- SD card

- 9 VDC, 1 A external power supply for use when LGR-5325 is not powered through the screw terminals

Optional components

ACC-202 Din-rail kit

Accessory for mounting a LGR-5325 to a standard DIN rail. Use the thread-forming screws to attach the DIN rail clip to your device.

Installing the software

Refer to the *DAQLog Software User's Guide* for instructions on installing and using the DAQLog software. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQLog-Software.pdf.

Installing the hardware

Follow these steps to provide power to the LGR-5325 and connect it to a USB port on your host computer.

Providing power to the LGR-5325

- To power the LGR-5325 from its screw terminals, connect the **PWR+** terminal to the positive lead of your power source, and the **PWR-** terminal to the negative lead of the power source. Use a power source that meets the power specifications of the LGR-5325.
- To power the LGR-5325 from an external power source, using the power connector, connect the 9 VDC, 1 A external power supply to the external power connector (see Figure 3 on page 11), and plug the adapter into an electrical outlet.

Always provide power to the LGR-5325 before connecting its USB cable to the computer

Connect the external power cable to the LGR-5325 before connecting the USB cable to the computer. This allows the LGR-5325 to inform the host computer (when the USB cable is connected) that the device requires minimal power from the computer's USB port.

Connecting the LGR-5325 to your system

To connect the LGR-5325 to your system, turn the computer on, and connect a USB cable from the LGR-5325's USB connector (see Figure 3 on page 11) to either a USB port on the computer or an external USB hub connected to the computer.

When you connect the LGR-5325 for the first time, a **Found New Hardware** message opens as the device is detected. When the message closes, the installation is complete.

Functional Details

LGR-5325 external components

The external components of the LGR-5325 shown in Figure 2 are explained in the following sections.

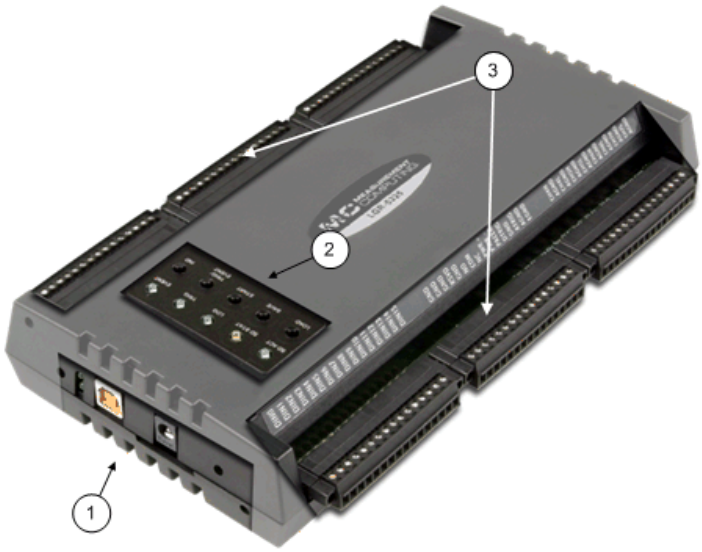

Figure 2. LGR-5325 external component locations

① USB and power connectors and LEDs, SD slot, and reset button.

② Function buttons and LEDs.

③ Screw terminals and LEDs

The components indicated by ① are identified in Figure 3 and explained below.

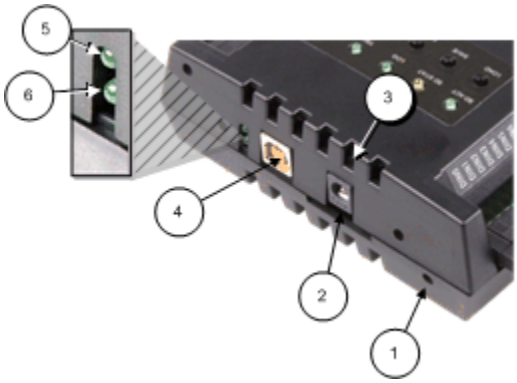

Figure 3. LGR-5325 connectors, SD card slot, LEDs, and reset button

① Recessed reset button – Use a ballpoint pen to push the button and reset device.

② SD card slot – The SD card slot accepts SD and SDHC memory cards. An SD card ships with the device.

③ External power supply connector (for use with 9 VDC power supply).

④ USB connector – Connect to an active USB port with USB cable

⑤ Power LED – Lit when the LGR-5325 is connected to a power source and ready for use.

⑥ USB activity LED – Lit when the LGR-5325 is connected to an active USB port.

Buttons and LEDs (top of case)

All buttons and LEDs on the top of the case are disabled when the LGR-5325 is connected to a USB port.

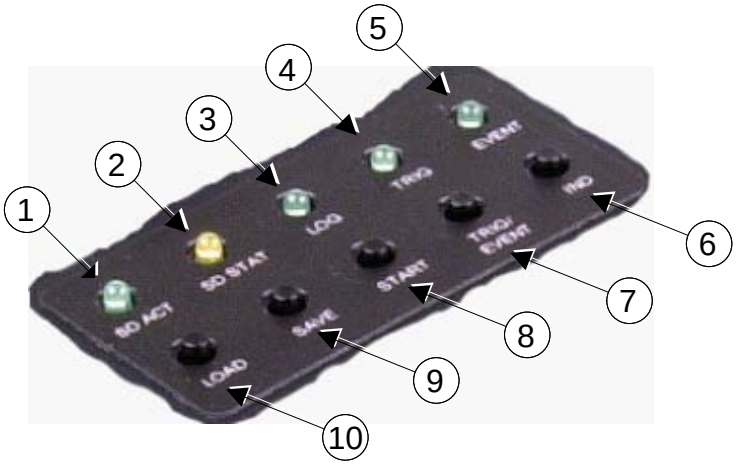

Figure 4. LGR-5325 LEDs and buttons (top of case)

① **SD ACT** LED – Blinks when data is read from or written to the SD card.

Caution! Do not remove the SD card when the **SD ACT** LED is blinking.

② **SD STAT** LED – Turns on for one second if you attempt an operation with no card in the slot.
Blinks when the device detects an error on the SD card or SD drive, or if the configuration file on the SD card is invalid.
The analog input LEDs on both screw terminals also blink when an error occurs, and the number blinking on each terminal indicate the error. Press any button on the top of the case to acknowledge the error and stop the LEDs from flashing.

For example, if you attempt to log without an SD card inserted in the LGR-5325, the **AGND** terminal at the end of one terminal strip blinks, and the **CH0H** on the other terminal strip blinks.
All SD STAT errors and corresponding analog input LED blink codes are explained below.

Error	**Analog input LED blink code**
Card not present	One analog LED blinks on each terminal
Card not mounted	Two analog LEDs on each terminal
Card write protected	Three analog LEDs on each terminal
File system error	Four analog LEDs on each terminal
FLASH write error	Five analog LEDs on each terminal
Overrun – pacer	Six analog LEDs on each terminal
Overrun – FIFO	Seven analog LEDs on each terminal
Overrun – events	Eight analog LEDs on each terminal
DMA error	Nine analog LEDs on each terminal
Card full	10 analog LEDs on each terminal
File reached max size	11 analog LEDs on each terminal
Log configuration error	12 analog LEDs on each terminal
Log configuration not valid for device	13 analog LEDs on each terminal

③ **LOG** LED - Solid when the LGR-5325 is logging. Off when the logger is idle.

④ **TRIG** LED – Turns on when the acquisition is triggered.

⑤ **EVENT** LED – Blinks when an event occurs.

⑥ **IND** button – Cycles through and selectively enables/disables LEDs with each button press. By default, all LEDs are enabled when the device is powered up.
If you press the button when the LEDs are in their default, only the LEDs on top of the device are enabled.
If you press the button again, all LEDs are disabled.
If you press the button again, all LEDs are enabled.

⑦ **TRIG/EVENT** button – Forces a trigger if logging has started and the device is waiting for a trigger. Adds an event to the event log if they are being recorded.

⑧ **START** button – Starts logging when an SD card with a valid configuration file is in the SD card slot, and the LGR-5325 is disconnected from a USB port. When the LGR-5325 is logging data, pressing this button stops the data logging.

⑨ **SAVE** button – Saves the current logging configuration to a file on the SD card.

⑩ **LOAD** button – Loads the latest logging configuration file from the SD card.

Figure 5. LOG and TRIG LEDS lit

Screw terminals and LED indicators

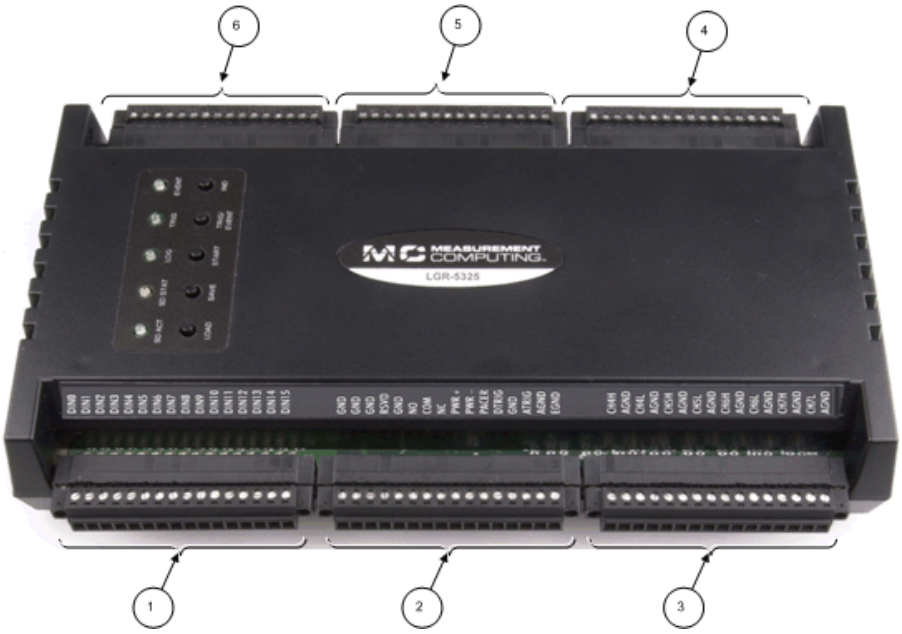

Figure 6. LGR-5325 front screw terminals and LEDs

① Digital input terminals and LEDs – LED for each active digital connection is on when voltage is detected.

② Digital trigger, pacer, digital, earth, and analog ground terminals, and digital output state LED – LED near **PWR+** terminal is on when the relay is energized, and off when the relay is de-energized.

③ Analog input 4–7, 12–15 (SE), 4–7 (Diff) terminals and LEDs – LED is on if channel is in the scan list.

④ Analog input 0–3, 8–11 (SE), 0–3 (Diff) terminals and LEDs – LED is on if channel is in the scan list, and off if channel is not in the scan list.

⑤ Counter input 0 and 1 terminals and LEDs – LED is on when the counter value is transitioning.

⑥ Counter input 2 and 3 terminals and LEDs – LED is on when the counter is transitioning.

Figure 7. Screw terminal LED lit

Analog input terminals

The LGR-5325 has a 16-bit, multiplexed A/D that supports up to 16 single-ended, or up to eight differential analog inputs.

The maximum throughput sample rate is 100 kS/s.

- Single-ended analog channels 0–3
  CH0H = channel 0 SE
  CH1H = channel 1 SE
  CH2H = channel 2 SE
  CH3H=channel 3 SE
- Differential analog channels 0–3
  CH0H /**CH0L** through **CH3H** /**CH3L**
- Single-ended analog channels 8–11
  CH0L = channel 8 SE
  CH1L = channel 9 SE
  CH2L = channel 10 SE
  CH3L = channel 11 SE
- Single-ended analog channels 4–7
  CH4H = channel 4 SE
  CH5H = channel 5 SE
  CH6H = channel 6 SE
  CH7H=channel 7 SE
- Single-ended analog channels 12–15
  CH4L = channel 12 SE
  CH5L = channel 13 SE
  CH6L = channel 14 SE
  CH7L = channel 15 SE
- Differential analog channels 4–7
  CH4H /**CH4L** through **CH7H** /**CH7L**

You can configure the LGR-5325's analog input channels for the following voltage input ranges:

- ±10 V
- ±5 V
- ±1 V

Unused analog input channels can either be left floating or connected to an **AGND** terminal block pin.

When connecting differential inputs to floating voltage sources in the ±10 V, ±5 V, or ±1 V ranges, you must provide a DC return path from each differential input to ground. You do this by connecting a resistor from the low terminal (**CHxL)** of each differential input to **AGND**. Use a value of approximately 100 kΩ for most applications.

The LGR-5325's **AGND** and **GND** terminals are tied together internally. These grounds are electrically isolated from the **EGND** (earth ground) terminal block pin.

Trigger terminals

The LGR-5325 supports the following trigger modes to accommodate certain measurement situations.

- External digital trigger
- External analog trigger (single-channel)
- Digital pattern trigger

You can always manually trigger an acquisition by pressing the **TRIG/EVENT** button when a triggered acquisition starts.

Digital and analog triggers connected

The input of the digital trigger and the output of the single-channel analog signal comparator are connected directly to hardware circuits to provide low-latency triggering. Latencies should be low (around 1.5 µs).

External digital trigger

A digital (or TTL-level) trigger starts an acquisition when the trigger condition is met at the **DTRIG** terminal.

When using digital triggering, the TTL trigger signal on the **DTRIG** connector is for a trigger condition. When the selected condition occurs, it is the trigger event.

If the LGR-5325 is ready for a trigger, then the trigger event occurs.

If the LGR-5325 is not ready due to one of the following reasons, the trigger is ignored:

- Incomplete configuration
- The device is finishing the previously triggered acquisition

The LGR-5325 does not indicate when a trigger is ignored.

External analog trigger (single-channel)

The input signal on the **ATRIG** terminal is compared to a programmable analog trigger level.

- If the analog input trigger condition is met, the LGR-5325 generates an internal trigger signal.
- If the LGR-5325 is ready for a trigger, then the trigger event occurs.
- If the LGR-5325 is not ready – due to incomplete configuration, or because the device is finishing the previously triggeredacquisition – the trigger is ignored.

The LGR-5325 does not indicate when a trigger is ignored.

Hysteresis

The analog trigger circuit has hysteresis to reduce the occurrence of false triggering due to input noise.

Hysteresis is the range that a signal must pass through before a trigger is generated. This prevents false triggers from happening when small amounts of noise exist on the signal.

Figure 8 shows the hysteresis effect for a rising-edge trigger.

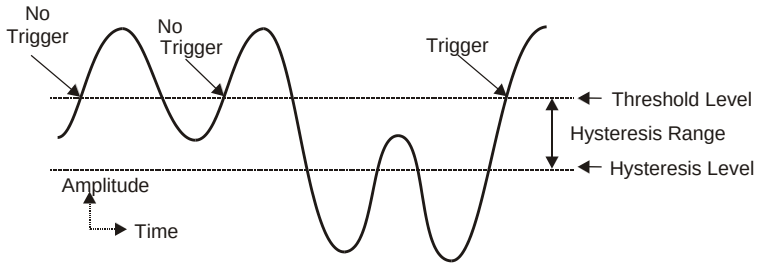

Figure 8. Hysteresis effect on a rising-edge trigger

A trigger occurs when the analog input rises above the trigger level, or *threshold* –but only after the input level has been below the hysteresis range. If the level briefly drops just below the threshold – perhaps due to noise – and then rises above it again, no extra triggers occur, since the signal did not drop below the hysteresis range.

After the level drops below hysteresis, it can then again produce a trigger by rising above the threshold.

Analog trigger types

Each trigger type is a combination of three elements: *slope*, *duration*, and *initialization*.

- **Slope** (above/rising or below/falling) – Sets whether the trigger is valid when the signal is *above the threshold* (rising) or *below the threshold* (falling).
- **Duration** (instantaneous or latched) – Specifies the action to take if the signal level becomes invalid after it has been valid:
  - *Instantaneous triggers* are valid in scans where that channel's trigger condition is met. They can become invalid in subsequent scans when the trigger condition is not met.
  - *Latched triggers* remain valid until the acquisition is complete. These trigger types are used to trigger scans when two or more signals have already become valid.
- **Initialization** (level or edge) – Specifies the sequence necessary for a signal to be a valid trigger/
  - *Level triggers* become valid as soon as they reach or exceed the threshold, even if they are already past the threshold when the acquisition starts.
  - Edge triggers first wait until the signal level is invalid. Then they wait for the signal to reach the threshold before becoming valid. Thus, level triggers look for a signal level, whenever it occurs; and edge triggers look for a rising or falling transition that reaches the threshold.

The first step in analog triggering is to examine the input signals. To determine trigger validity, the FPGA can examine each input signal in one of eight ways.

Trigger type	Slope	Duration	Initialization
Above-level	N/A	Instantaneous	Level
Below-level	N/A	Instantaneous	Level
Above-level-with-latch	N/A	Latched	Level
Below-level-with-latch	N/A	Latched	Level
Rising-edge	Rising	Instantaneous	Edge
Falling-edge	Falling	Instantaneous	Edge
Rising-edge-with-latch	Rising	Latched	Edge
Falling-edge-with-latch	Falling	Latched	Edge

The input signals are compared to a specified signal level.

Above-level trigger

This trigger is valid whenever the signal goes above the specified level, and stays valid until the signal goes below the level.

In Figure 9, the channel trigger is valid during the shaded intervals.

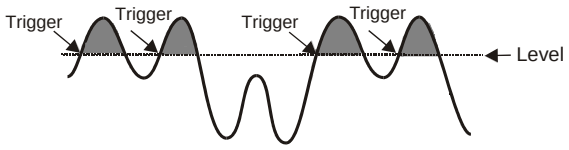

Figure 9. Above level initialization, instantaneous duration

Below-level trigger

This trigger is valid whenever the signal level is below the level and stays valid until the signal goes above the level – the opposite of above-level triggering.

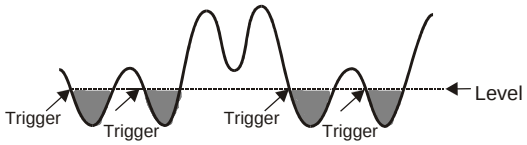

Figure 10. . Below level initialization, instantaneous duration

Above-level-with-latch trigger

With this trigger type, the channel becomes valid when the signal level is above the threshold, and remains valid until the acquisition is complete and re-armed.

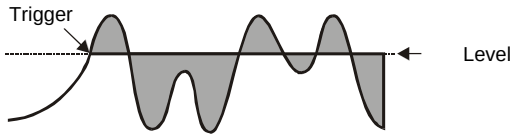

Figure 11. Above level initialization, latched duration

Below-level-with-latch trigger

With this trigger type, the channel becomes valid when the signal level is below the threshold and remains valid until the acquisition is complete and re-armed – the opposite of above-level-with-latch triggering).

If the trigger is not latched, the channel may not stay valid. The LGR-5325 will not trigger the acquisition until the channel becomes valid again, and all channels simultaneously reach their thresholds.

Latched triggering is used to trigger an acquisition after an event has occurred, while non-latched triggering is used only during the simultaneous occurrence of desired signal levels.

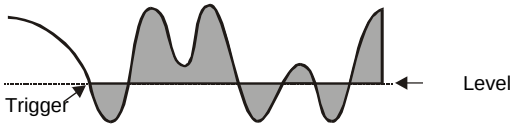

Figure 12. Below level initialization, latched duration

Rising-edge trigger

This trigger becomes valid after the signal level has been below the hysteresis range and then goes above the threshold. This trigger becomes invalid when the signal level goes below the hysteresis range. Unlike above-level triggering, the channel cannot become valid until the signal level first goes below the hysteresis range. This prevents the false triggering that would occur if the signal were above the threshold at the start of the acquisition.

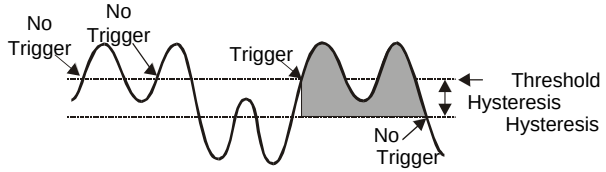

Figure 13: Rising edge, instantaneous duration, edge initialization

Falling-edge trigger

This trigger is the reverse of the rising-edge trigger: the trigger becomes valid after the signal level has been above the hysteresis range and then goes below the threshold. This trigger becomes invalid whenever the signal level goes above the hysteresis range. This prevents the false triggering that would occur with below-level triggering if the signal was below the threshold at the start of the acquisition.

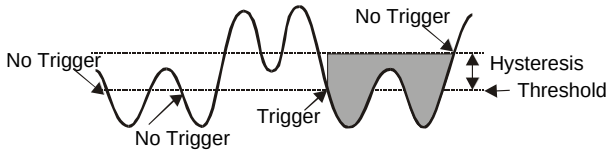

Figure 14: Falling slope, instantaneous duration, edge initialization

Rising-edge-with-latch trigger

This trigger becomes valid like a rising-edge trigger – when the signal level goes above the threshold after first being below the hysteresis range. However, the rising-edge-*with-latch* trigger does not become invalid, regardless of the signal level, until the acquisition is complete. Rising-edge-with-latch is used to trigger after the channel has reached the threshold, rather than just while the channel is above the threshold.

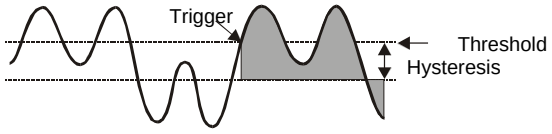

Figure 15: Rising slope, latched duration, edge initialization

Falling-edge-with-latch trigger

This trigger is the reverse of the rising-edge-with-latch trigger – it becomes valid after the signal level has been above the hysteresis range and then goes below the threshold. The trigger remains valid until the acquisition is complete.

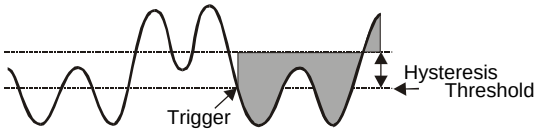

Figure 16: Falling slope, latched duration, edge initialization

Digital-pattern trigger

The digital pattern trigger is an expanded digital-trigger that starts collecting data when a 1 to 16-bit digital pattern – that you define with *pattern* and *mask* parameters – matches the bit pattern on the digital input connector.

This type of trigger is useful when trying to capture noise, vibrations, or some other physical disturbance that occurs at a particular point in a digitally-sequenced process, such as a relay-logic-control system.

Two parameters control this trigger operation – the *condition* and the *mask*.

- The *polarity* parameter allows the following choices:
  - **Rising edge/high level (equal to)** – Triggers when there is an exact pattern matches of "1s" and "0s" between the compared patterns.
  - **Falling edge/low level (not equal to)** – Triggers on any change of "1s" and "0s" between two patterns that previously matched.
- The *mask* parameter can set any of the input bits to "don't care" (X), which excludes that bit from the polarity comparison.

Digital input and output terminals

You can connect up to 16 digital inputs to the LGR-5325. Each digital input is electrically isolated from the host PC and from the LGR-5325's analog and counter circuits.

You can configure these inputs to detect events based on change of state or pattern recognition. These are the same bits used for a digital pattern trigger (see the "Digital-pattern trigger" section above)

The digital inputs have a wide input voltage range of 0 to +30 V.

The digital output is an alarm implemented as a single Form C relay on the **NC** (normally closed), **COM** (common), and **NO** (normal open) screw terminals.

You can configure the relay to energize when the trigger condition is met and data is being recorded.

Always use the GND screw terminals with digital inputs

Always use the GND screw terminals as the ground return for digital inputs.

Counter input terminals and modes

The LGR-5325 supports the following counter input modes:

- Counter (general event counting)
- Period counting
- Pulse width counting
- Edge-to-edge timing
- Up/down counting

You can use the Modulo N number and mode with all of the counter modes listed to determine how the counter behaves when it reaches the *modulo* number you set.

The LGR-5325 can read counter inputs as part of a digital scan group.

When read as part of a scan, the count of each channel's counter is set to 0 and latched at the beginning of the synchronous acquisition. Each clock pulse (*start-of-scan* signal) initiates a scan of all channels specified. Each time the LGR-5325 receives a *start-of-scan* signal, the counter values are latched and are available to the device. The values returned during scan period 1 are always zero. The values returned during scan period 2 reflect what happened during scan period 1. The scan period defines the timing resolution. To achieve a higher timing resolution, shorten the scan period.

Counter operation modes are programmable with software. Some modes use the user-configurable *modulo* number. This number does not directly affect the current count, but sets a limit used in some modes to determine counter behavior.

All counter modes use the **CTRx** input. Some modes also make use of the **UPDNx** and **GATEx** inputs.

Each mode supports additional sub-modes for counter operations. Refer to the discussion of each counter mode in the pages that follow for specific information.

Counter mode

You can use the LGR-5325 as a high-speed pulse counter for general counting applications.

Each counter is a 32-bit counter, and accepts frequency inputs up to 10 MHz.

In counter mode, **CTRx** is the primary counter input. You can use **UPDNx** to set the count direction in up/down counting. Use the **GATEx** input to gate, latch, or decrement the counter.

The LGR-5325 reads counter inputs synchronously as part of the scan list, and supports the following options in counter mode:

Counter mode options

Counter mode	Description
Totalize	General pulse counter.
Clear on read	The counter clears after each synchronous read. The counter value is latched and returned before it clears.

Modulo mode options (Counter mode)

Counter mode	Description
Range limit	When counting up: The counter stops when the maximum count (specified by the *modulo* number) is reached. Counting resumes if the direction reverses or the counter reloads. When counting down: The counter will count down to 0 and then stop. Counting resumes if direction reverses or the counter reloads.
Non-recycle	The counter is disabled if a count overflow or underflow occurs or the *modulo* number is reached. A clear command (via software or **GATEx** input) is required to re-enable the counter.
Up/down	Up/down counting mode uses **CTRx** as the pulse source and **UPDNx** as the direction. The counter counts up when **UPDNx**=1 (high), and counts down when **UPDNx** =0 (low).
Modulo-N	Sets the specified *modulo* number used by the counter mode options explained in this table.

Some counter mode options are specific to the **GATEx** signal. These modes are explained in the following table.

GATEx input mode options (counter mode)

GATEx mode	Description
Gating	Gating mode allows the **GATEx** input to gate the counter. The counter is enabled when the **GATEx** signal is high. When the **GATEx** signal is low, the counter is disabled, but holds the count value.
Latching	Latching mode allows the **GATEx** signal to latch the count.
Decrement	Decrement mode allows the **GATEx** signal to decrement the counter.

Period measurement mode

Use period mode to measure the period of a signal at a counter channel's **CTRx** input. You can measure 1X, 10X, 100X or 1000X periods, 16-bit or 32-bit values. Four resolutions are available – to 20 ns, 200 ns, 2 µs, or 20 µs. All period measurement mode options are software-selectable. The LGR-5325 uses the 50 MHz system clock as the timing source. The LGR-5325 measures periods from sub-microsecond to many seconds.

The LGR-5325 reads counter channel inputs synchronously using period mode.

Pulse width measurement mode

Use pulse width mode to measure the time from the rising edge to the falling edge--or vice versa--on a signal on a **CTRx** counter input. Four resolutions are available (20 ns, 200 ns, 2 µs, or 20 µs). All pulse width measurement mode options are software selectable. The LGR-5325 uses the 50 MHz system clock as the timing source. Pulse widths from sub-microsecond to many seconds can be measured.

The LGR-5325 reads counter channel inputs synchronously using pulse width mode.

Timing measurement mode

Measures the time from a rising or falling edge on **CTRx** to a rising or falling edge on **GATEx**.

Debounce mode

The LGR-5325 has debounce circuitry, which eliminates switch-induced transients that are typically associated with electromechanical devices including relays and proximity switches.

All debounce options are software selectable. You can select a debounce time, debounce mode, and rising-edge or falling-edge sensitivity. The LGR-5325 can debounce each channel with 16 programmable debounce times in the range of 500 ns to 25.5 ms.

Two debounce modes (*trigger after stable* and *trigger before stable*) and a debounce bypass are shown in Figure 17. The signal from the buffer can be inverted before it enters the debounce circuitry. The inverter makes the input rising-edge or falling-edge sensitive.

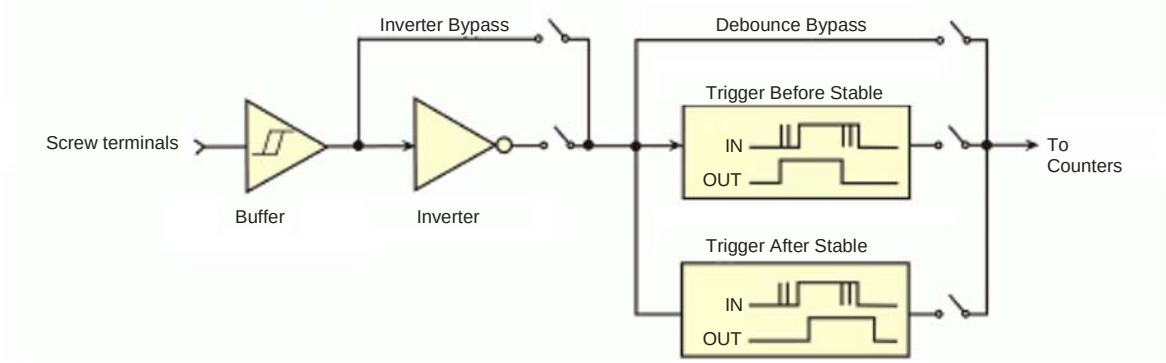

Figure 17. Debounce block diagram

Edge selection is available with or without debounce. In this case, the debounce time setting is ignored and the input signal goes straight from the inverter or inverter bypass to the counter module.

The two debounce modes are *trigger after stable* and *trigger before stable*. In either mode, the selected debounce time determines how fast the signal can change and still be recognized.

Trigger after stable mode

In the *trigger after stable* mode, the output of the debounce module does not change state until a period of stability has been achieved. This means that the input has an edge, and then must be stable for a period of time equal to the debounce time. Refer to Figure 18.

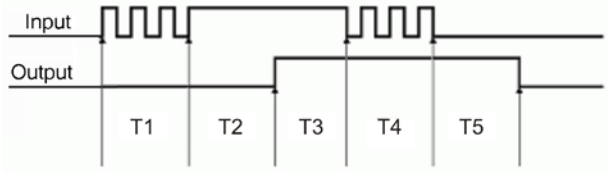

Figure 18. *Trigger after stable* mode

T1 through T5 indicate time periods. In *trigger after stable* mode, in order for that edge to be accepted (passed through to the counter module), the input signal to the debounce module is required to have a period of stability after an incoming edge. For this example, the debounce time is equal to T2 and T5.

- T1 – In Figure 18, the input signal goes high at the beginning of time period T1, but never stays high for a period of time equal to the debounce time setting (equal to T2 for this example.)
- T2 – At the end of time period T2, the input signal has transitioned high and stayed there for the required amount of time – therefore the output transitions high. If the input signal does not stabilize in the high state long enough, no transition would have appeared on the output, and the entire disturbance on the input would have been rejected.
- T3 – During time period T3, the input signal remained steady. No change in output is seen.
- T4 – During time period T4, the input signal has more disturbances and does not stabilize in any state long enough. No change in the output is seen.
- T5 – At the end of time period T5, the input signal has transitioned low and stayed there for the required amount of time – therefore the output goes low.

Trigger before stable mode

In the *trigger before stable* mode, the output of the debounce module immediately changes state, but does not change again until a period of stability has passed. For this reason, you can use this mode to detect glitches. Refer to Figure 19.

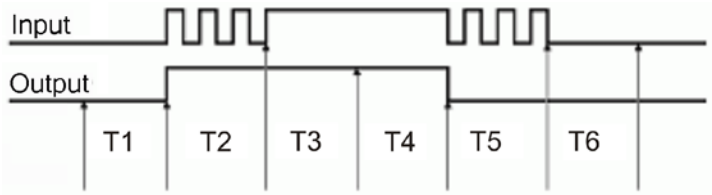

Figure 19. *Trigger before stable* mode

"T1" through "T5" in Figure 19 indicates time periods:

- T1 – The input signal is low for the debounce time (equal to T1); therefore, when the input edge arrives at the end of time period T1, it is accepted and the output (of the debounce module) goes high. Note that a period of stability must precede the edge in order for the edge to be accepted.
- T2 – During time period T2, the input signal is not stable for a length of time equal to T1 (the debounce time setting for this example.) Therefore, the output stays "high" and does not change state during time period T2.
- T3 – During time period T3, the input signal is stable for a time period equal to T1, meeting the debounce requirement. The output is held at the high state. This is the same state as the input.
- T4 – At anytime during time period T4, the input can change state. When this happens, the output will also change state. At the end of time period T4, the input changes state, going low, and the output follows this action [by going low].
- T5 – During time period T5, the input signal again has disturbances that cause the input to not meet the debounce time requirement. The output does not change state.
- T6 – After time period T6, the input signal has been stable for the debounce time and therefore any edge on the input after time period T6 is immediately reflected in the output of the debounce module.

Debounce mode comparisons

Figure 20 shows how the two modes interpret the same input signal, which exhibits glitches. Notice that the *trigger before stable* mode recognizes more glitches than the *trigger after stable* mode. Use the **bypass** option to achieve maximum glitch recognition.

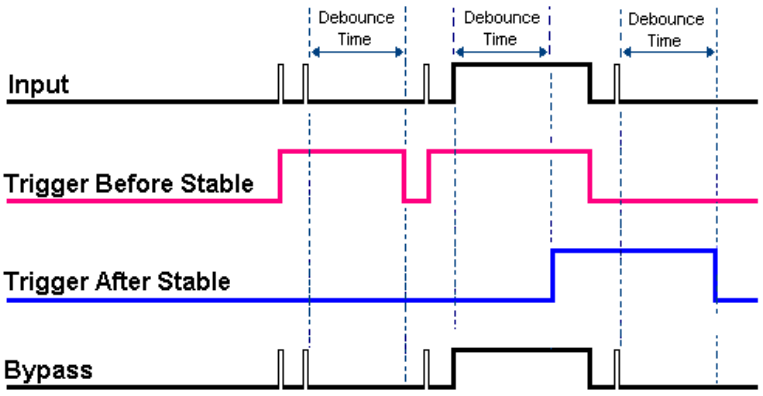

Figure 20. Example of two debounce modes interpreting the same signal

Set the debounce time according to the amount of instability expected in the input signal. Setting a debounce time that is too short may result in unwanted glitches clocking the counter. Setting a debounce time that is too long may result in an input signal being rejected entirely. Some experimentation may be required to find the appropriate debounce time for a particular application.

To see the effects of different debounce time settings, view the analog waveform along with the counter output. You can do this by connecting the source to an analog input.

Use *trigger before stable* mode when the input signal has groups of glitches and each group is to be counted as one. The *trigger before stable* mode recognizes and counts the first glitch within a group, but rejects the subsequent glitches within the group if the debounce time is set accordingly. Set the debounce time to encompass one entire group of glitches, as shown in Figure 21.

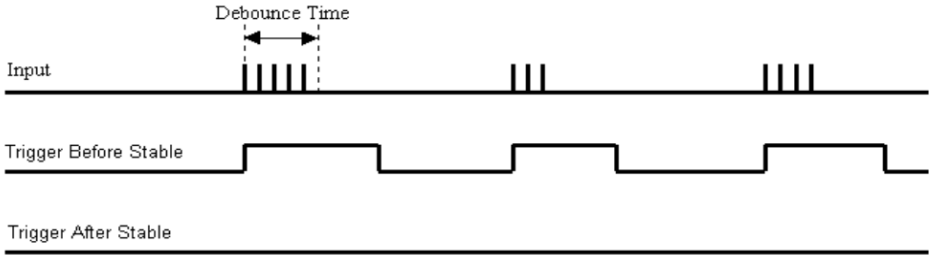

Figure 21. Optimal debounce time for *trigger before stable* mode

Trigger after stable mode behaves more like a traditional debounce function: rejecting glitches and only passing state transitions after a required period of stability. Use *Trigger after stable* with electromechanical devices like mechanical switches to reject switch bounce and disturbances due to a vibrating encoder that is not otherwise moving. The debounce time should be set short enough to accept the desired input pulse, but longer than the period of the undesired disturbance, as shown in Figure 22.

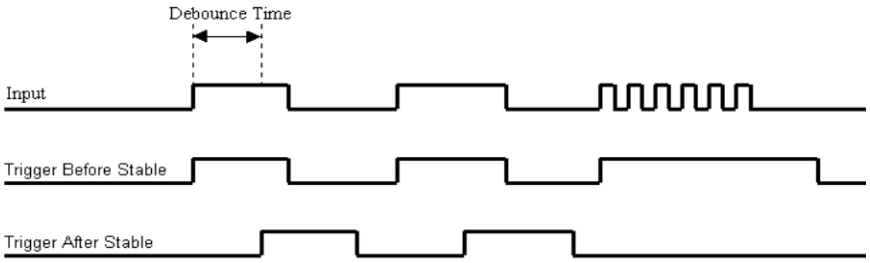

Figure 22. Optimal debounce time for *trigger after stable* mode

Mechanical drawings

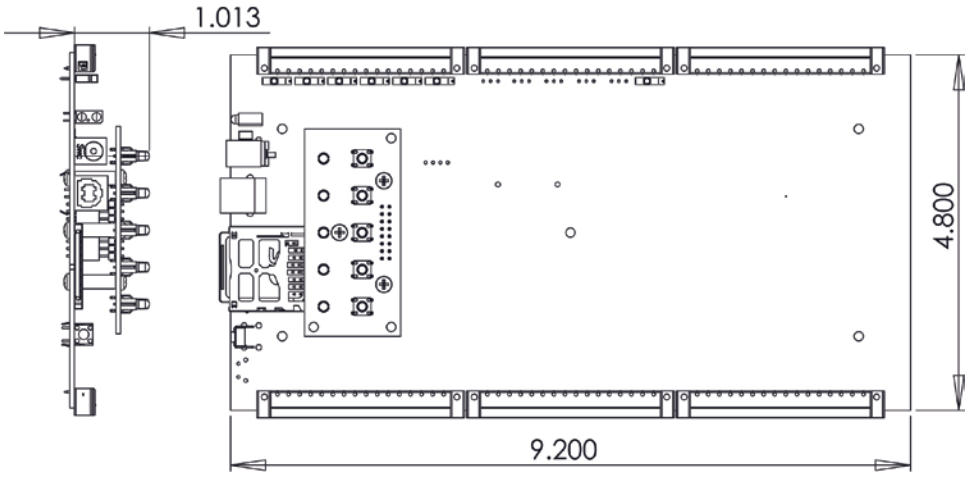

Figure 23. Circuit board dimensions

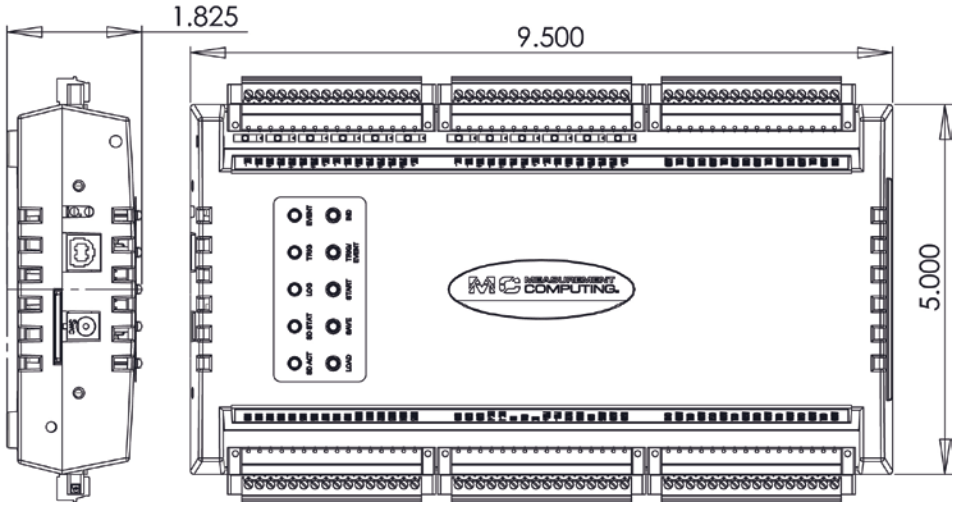

Figure 24. Housing dimensions

Specifications

All specifications are subject to change without notice.
Typical for 25 °C unless otherwise specified.
Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

Parameter	Condition	Specification
A/D converter		16-bit successive approximation type
Input ranges	Software selectable per channel	±10 V, ±5 V, ±1 V
Number of channels		8 differential/16 single-ended, software configurable
Input configuration		Multiplexed
Absolute maximum input voltage	*CHx_x to AGND*	*±25 V maximum(power on and power off)*
Input impedance	*±10 V, ±5 V, ±1 V range*	*10 GΩ (power ON)* *1 kΩ (power OFF)*
Input leakage current		*±100 pA*
Input capacitance	±10 V, ±5 V, ±1 V ranges	*55 pf*
Maximum working voltage (signal + common mode)	±10 V, ±5 V, ±1 V ranges	±10.2 V
Common mode rejection ratio	fin = 60 Hz	75 dB minimum
Crosstalk	DC to 25 kHz, adjacent differential mode channels	–80 dB
ADC resolution		16 bits
Input bandwidth (–3 dB)	All input ranges	450 kHz minimum
Input coupling		DC
Maximum sampling rate		100 kHz
A/D pacing sources		See input sequencer section
Warm up time		30 minutes, minimum
Absolute accuracy	All ranges	0.07% FSR
Noise	Differential mode	2 LSB rms

Note 1: Unused analog input channels can either be left floating or tied to an AGND pin.

Note 2: When connecting differential inputs to floating voltage sources in the ±10 V, ±5 V, ±1 V ranges, the user must provide a DC return path from each differential input to ground. To do this, simply connect a resistor from each of the differential inputs to AGND. A value of approximately 100 kΩ can be used for most applications.

Note 3: The AGND and GND pins are tied together internally. These grounds are electrically isolated from the EGND (earth ground) pin.

Analog input calibration

Table 2. Analog input calibration specifications

Parameter	Specifications
Calibration method	Factory calibration
Calibration interval	1 year

External clock input

Table 3. External clock I/O specifications

Parameter	Condition	Specification
External clock I/O		PACER (pin 75), software programmable as input or output
Input high voltage		2.2 V maximum
Input low voltage		0.6 V minimum
Output high voltage	IOH = –8 mA	3.8 V minimum
Output low voltage	IOL = 8 mA	0.4 V maximum
Pacer rate		100 kHz maximum
Minimum pulse width		2.5 us minimum

Input sequencer

Table 4. Input sequencer specifications

Parameter	Specifications
Pacer clock sources: two	▪ Internal: From 10 µs to 85.9 sec in 20 ns steps ▪ External (PACER): 10 µs minimum
Programmable parameters per scan	▪ Channel type (differential analog, single ended analog, counter, digital input) ▪ Channel number (random order) ▪ Gain
Depth	512 locations
Pacer interval	10 µs minimum (100 kHz maximum pacer rate)
Channel to channel sampling period (scan clock)	▪ 10 µs, fixed (analog inputs) ▪ All specified digital channels (counters, digital inputs) are sampled simultaneously at the beginning of the pacer interval

Triggering

Table 5. Triggering specifications

Parameter	Condition	Specification
Mode	External digital via DTRIG (pin 76)	Software configurable for rising or falling edge.
	External analog via ATRIG (pin 78)	See Table 6
External digital trigger latency	Non-pretrigger acquisition	100 ns typical, 1 µs maximum
	Pretrigger acquisition	1 scan period maximum
External trigger pulse width		1 µs minimum
Internal trigger latency		2* (1/per-channel sample rate)

External analog trigger

Table 6. External trigger specifications

Parameter	Conditions	Specification
External analog trigger source		ATRIG input (pin 78)
Analog trigger input range		±10 V
Absolute maximum input voltage	*ATRIG_IN to AGND*	*±25 V maximum (power on and power off)*
Input impedance	*±10 V range*	*10 GΩ (power ON)* *1 kΩ (power OFF)*
Trigger modes		Configurable for: ▪ Positive or negative slope ▪ Level
Trigger/Hysteresis resolution		12 bits, 1 in 4096
Trigger/Hysteresis levels		±10 V/4096 software configurable
Trigger/Hysteresis accuracy		±2% of reading, ±50 mV offset
Latency		1.5 µS
Full power bandwidth (–3 dB)		1 MHz

Digital input

Table 7. Digital Input specifications

Parameter	Specification
Number of inputs	16 channels
Input voltage range	0 to +28 V
Input type	TTL
Input characteristics	47 kΩ pull-down resistor, 39.2 kΩ series resistor
Maximum input voltage level	+32 V (power on/off)
Minimum high level input voltage threshold	2.0 V maximum
Maximum low level input voltage threshold	0.8 V minimum

Digital output

Table 8. Digital Output specifications

Parameter	Specification
Number of outputs	1
Type	Mechanical relay, NEC ED2/EF2 series
Relay configuration	1 Form C
Relay contact resistance	0.075 Ω
Relay contact operate time	3 mS (excluding bounce)
Relay contact release time	2 ms (excluding bounce)
Relay insulation resistance	1000 MΩ at 500 VDC
Relay contact ratings	Maximum switching voltage: 220 VDC/250 VAC
	Maximum switching current: 1.0 A
	Maximum carrying current: 2.0 A

Fault tolerance

Table 9. Fault condition behavior

Condition	Behavior
Power loss	▪ Volatile memory data loss (internal memory) ▪ Data loss if data being written to non-volatile storage. MCC cannot guarantee the integrity of existing data on the storage device. (Note 4)
Unexpected removal of SD card	▪ Data loss if data being written to non-volatile storage. MCC cannot guarantee the integrity of existing data on the storage device. (Note 4)
Power on after fault	▪ Unit will restart with existing configuration.

Note 4: Solid-state memory devices behave differently under fault conditions. MCC cannot guarantee the integrity of data, both new and existing, in the event of power loss, unexpected media removal, or similar actions.

Counters

Table 10. Counter specifications

Parameter	Condition	Specification
Counter type		Conventional
Number of channels		4
Inputs		Counter, Up/Down, Gate
Resolution		Fixed 32-bit or as sized by the modulo register.
Count Modes		Up/down counting
		Period/frequency counting
		Modulo-N
De-bounce times (programmable)		16 steps from 500 ns to 25 ms; positive or negative edge sensitive; glitch detect mode or de-bounce mode
Time-base accuracy		50 ppm
Input voltage range		0 to 5.5 V
Input type		TTL
Input characteristics		49.9 kΩ pull-down resistor
Maximum input voltage range		–0.5 V to +7.0 V
Input high voltage		2.0 V
Input low voltage		0.8 V

Device configuration

Table 11. Configuration

Parameter	Specification
Local	Host PC over USB
Remote	Via configuration file on SD card
Configuration file format	Binary

Controls/indicators

Table 12. Controls/indicators

Parameter	Specification
LOAD button	Loads a configuration from the SD card/enters USB boot loader (hold while applying power)
SAVE button	Saves configuration to the SD card
START button	Starts an acquisition
TRIG/EVENT button	Forces a trigger/logs an event
IND button	Turns LED indicators on/off in 3 steps: All on – Top indicators only – All off
Reset button	Resets the device
SD ACT indicator	Indicates SD card read/write activity
SD STAT indicator	Indicates SD card/device error condition if blinking
LOG indicator	Indicates acquisition in progress
TRIG indicator	Indicates trigger occurred
EVENT indicator	Flashes when an event is logged or configuration is loaded or saved
Power indicator	(Top LED on case end.) Indicates power is good and device is ready
USB indicator	(Bottom LED on case end.) Indicates USB connection is active; blinks off for USB activity.
Analog input indicators	Indicates corresponding analog input is in the acquisition
Digital input indicators	Indicates presence of a voltage at the corresponding digital input pin (not necessarily a high logic level)
Digital output indicator	Indicates relay state
Counter input indicators	Indicates corresponding counter activity

Data Memory

Table 13. Data Memory

Parameter	Specification
Supported removable media	Secure Digital (SD), Secure Digital High Capacity (SDHC)
Data file format	Binary. Data time stamped using real-time clock.

Power

Table 14. Power specifications

Parameter	Condition	Specification
External power input		PWR+ (pin 73)/PWR– (pin 74) +9 VDC minimum +30 VDC maximum
External power supply		+9 VDC minimum +30 VDC maximum
Power supply fuse	0157002.DRT. - Littelfuse 2A NANO$^{2®}$ Slo-Blo® Subminiature surface mount fuse	
Power supply current	+9 VDC input, continuous logging mode	225 mA typical, 630 mA maximum
	+30 VDC input, continuous logging mode	100 mA typical, 210 mA maximum

Note 5: The AGND and GND pins are tied together internally. These grounds are electrically isolated from the EGND (earth ground) pin.

Chassis ground

Table 15. Chassis ground specifications

Parameter	Specification
Number of inputs	Single terminal EGND (pin 80)
Isolation method	10 nF/1000 V ceramic capacitor in parallel with 1 MΩ resistor

Note 6: The EGND pin is isolated from the measurement and I/O circuits. The EGND pin should only be used to connect the LGR-5325 to a local chassis ground connection and should not be used as a return path for any of the analog or digital I/O.

USB specifications

Table 16. USB specifications

Parameter	Specification
USB device type	USB 2.0 (full-speed)
USB device compatibility	USB 1.1, 2.0
USB cable length	3 meters maximum.
USB cable type	A-B cable, UL type AWM 2527 or equivalent

Environmental

Table 17. Environmental specifications

Parameter	Specification
Operating temperature range	0 to 55 °C
Storage temperature range	–40 to 85 °C
Humidity	0 to 90% non-condensing

Mechanical

Table 18. Mechanical specifications

Parameter	Specification
Dimensions	9.5" L x 5.0" W x 1.75" H
Mechanical shock (operating)	▪ 50 g, 3 ms half sine ▪ 30 g, 11 ms half sine Three hits per face for a total of 18 hits (18 hits at 50 g, 18 hits at 30 g) Test procedure: IEC 60068-2-27
Random vibration (operating)	10-500 Hz: 5 g_{rms} Test time: 100 minutes/axis Test procedure: IEC 60068-2-64

Screw terminal connector type

Table 19. Screw terminal connector specifications

Connector type	Detachable type
Wire gauge range	16 AWG to 30 AWG

Screw terminal pinout

Table 20. 8-channel differential mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	CH0H	Channel 0 HI	96	AGND	Analog ground
2	AGND	Analog ground	95	CH7L	Channel 7 LO
3	CH0L	Channel 0 LO	94	AGND	Analog ground
4	AGND	Analog ground	93	CH7H	Channel 7 HI
5	CH1H	Channel 1 HI	92	AGND	Analog ground
6	AGND	Analog ground	91	CH6L	Channel 6 LO
7	CH1L	Channel 1 LO	90	AGND	Analog ground
8	AGND	Analog ground	89	CH6H	Channel 6 HI
9	CH2H	Channel 2 HI	88	AGND	Analog ground
10	AGND	Analog ground	87	CH5L	Channel 5 LO
11	CH2L	Channel 2 LO	86	AGND	Analog ground
12	AGND	Analog ground	85	CH5H	Channel 5 HI
13	CH3H	Channel 3 HI	84	AGND	Analog ground
14	AGND	Analog ground	83	CH4L	Channel 4 LO
15	CH3L	Channel 3 LO	82	AGND	Analog ground
16	AGND	Analog ground	81	CH4H	Channel 4 HI
17	RSVD	Reserved	80	EGND	Chassis ground
18	CTR0	Counter 0 input	79	AGND	Analog ground
19	RSVD	Reserved	78	ATRIG	Analog trigger input
20	UPDN0	Up/down 0 input	77	GND	Digital ground
21	RSVD	Reserved	76	DTRIG	Digital trigger
22	GATE0	Gate 0 input	75	PACER	Pacer I/O
23	RSVD	Reserved	74	PWR–	Input ground
24	GND	Digital ground	73	PWR+	Input power
25	RSVD	Reserved	72	NC	Relay normally closed contact
26	CTR1	Counter 1 input	71	COM	Relay common contact
27	RSVD	Reserved	70	NO	Relay normally open contact
28	UPDN1	Up/down 1 input	69	GND	Digital ground
29	RSVD	Reserved	68	RSVD	Reserved
30	GATE1	Gate 1 input	67	GND	Digital ground
31	RSVD	Reserved	66	GND	Digital ground
32	GND	Digital ground	65	GND	Digital ground
33	RSVD	Reserved	64	DIN15	Digital input 15
34	CTR2	Counter 2 input	63	DIN14	Digital input 14
35	RSVD	Reserved	62	DIN13	Digital input 13
36	UPDN2	Up/down 2 input	61	DIN12	Digital input 12
37	RSVD	Reserved	60	DIN11	Digital input 11
38	GATE2	Gate 2 input	59	DIN10	Digital input 10
39	RSVD	Reserved	58	DIN9	Digital input 9
40	GND	Digital ground	57	DIN8	Digital input 8
41	RSVD	Reserved	56	DIN7	Digital input 7
42	CTR3	Counter 3 input	55	DIN6	Digital input 6
43	RSVD	Reserved	54	DIN5	Digital input 5
44	UPDN3	Up/down 3 input	53	DIN4	Digital input 4
45	RSVD	Reserved	52	DIN3	Digital input 3
46	GATE3	Gate 3 input	51	DIN2	Digital input 2
47	RSVD	Reserved	50	DIN1	Digital input 1
48	GND	Digital ground	49	DIN0	Digital input 0

Table 21. 16-channel single-ended mode pinout

Pin	Signal name	Pin description	Pin	Signal name	Pin description
1	CH0	Channel 0	96	AGND	Analog ground
2	AGND	Analog ground	95	CH15	Channel 15
3	CH8	Channel 8	94	AGND	Analog ground
4	AGND	Analog ground	93	CH7	Channel 7
5	CH1	Channel 1	92	AGND	Analog ground
6	AGND	Analog ground	91	CH14	Channel 14
7	CH9	Channel 9	90	AGND	Analog ground
8	AGND	Analog ground	89	CH6	Channel 6
9	CH2	Channel 2	88	AGND	Analog ground
10	AGND	Analog ground	87	CH13	Channel 13
11	CH10	Channel 10	86	AGND	Analog ground
12	AGND	Analog ground	85	CH5	Channel 5
13	CH3	Channel 3	84	AGND	Analog ground
14	AGND	Analog ground	83	CH12	Channel 12
15	CH11	Channel 11	82	AGND	Analog ground
16	AGND	Analog ground	81	CH4	Channel 4
17	RSVD	Reserved	80	EGND	Chassis ground
18	CTR0	Counter 0 input	79	AGND	Analog ground
19	RSVD	Reserved	78	ATRIG	Analog trigger input
20	UPDN0	Up/down 0 input	77	GND	Digital ground
21	RSVD	Reserved	76	DTRIG	Digital trigger
22	GATE0	Gate 0 input	75	PACER	Pacer I/O
23	RSVD	Reserved	74	PWR–	Input ground
24	GND	Digital ground	73	PWR+	Input power
25	RSVD	Reserved	72	NC	Relay normally closed contact
26	CTR1	Counter 1 input	71	COM	Relay common contact
27	RSVD	Reserved	70	NO	Relay normally open contact
28	UPDN1	Up/down 1 input	69	GND	Digital ground
29	RSVD	Reserved	68	RSVD	Reserved
30	GATE1	Gate 1 input	67	GND	Digital ground
31	RSVD	Reserved	66	GND	Digital ground
32	GND	Digital ground	65	GND	Digital ground
33	RSVD	Reserved	64	DIN15	Digital input 15
34	CTR2	Counter 2 input	63	DIN14	Digital input 14
35	RSVD	Reserved	62	DIN13	Digital input 13
36	UPDN2	Up/down 2 input	61	DIN12	Digital input 12
37	RSVD	Reserved	60	DIN11	Digital input 11
38	GATE2	Gate 2 input	59	DIN10	Digital input 10
39	RSVD	Reserved	58	DIN9	Digital input 9
40	GND	Digital ground	57	DIN8	Digital input 8
41	RSVD	Reserved	56	DIN7	Digital input 7
42	CTR3	Counter 3 input	55	DIN6	Digital input 6
43	RSVD	Reserved	54	DIN5	Digital input 5
44	UPDN3	Up/down 3 input	53	DIN4	Digital input 4
45	RSVD	Reserved	52	DIN3	Digital input 3
46	GATE3	Gate 3 input	51	DIN2	Digital input 2
47	RSVD	Reserved	50	DIN1	Digital input 1
48	GND	Digital ground	49	DIN0	Digital input 0

CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
Suite 1008
Norton, MA 02766
USA

Category:Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

LGR-5325

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EC EMC Directive 2004/108/EC: General Requirements, EN 61326-1:2006 (IEC 61326-1:2005).

Emissions:

- EN 55011 (2007) / CISPR 11(2003): Radiated emissions: Group 1, Class A
- EN 55011 (2007) / CISPR 11(2003): Conducted emissions: Group 1, Class A

Immunity: EN 61326-1:2006, Table 3.

- IEC 61000-4-2 (2001): Electrostatic Discharge immunity.
- IEC 61000-4-3 (2002): Radiated Electromagnetic Field immunity.
- IEC 61000-4-4 (2004): Electric Fast Transient Burst Immunity.
- IEC 61000-4-5 (2001): Surge Immunity.
- IEC 61000-4-6 (2003): Radio Frequency Common Mode Immunity.
- IEC 61000-4-11 (2004): Voltage Interrupts.

To maintain compliance to the standards of this declaration, the following conditions must be met.

- The host computer, peripheral equipment, power sources, and expansion hardware must be CE compliant.
- All I/O cables must be shielded, with the shields connected to ground.
- I/O cables must be less than 3 meters (9.75 feet) in length.
- The host computer must be properly grounded.
- Equipment must be operated in a controlled electromagnetic environment as defined by Standards EN 61326-1:2006, or IEC 61326-1:2005.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in October, 2009. Test records are outlined in Chomerics Test Report #EMI5475.09. Further testing was conducted by Chomerics Test Services, Woburn, MA. 01801, USA in April, 2010. Test records are outlined in Chomerics Test Report #TR5397.10.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja, Director of Quality Assurance

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